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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application No.: 10/057,393
Filed: January 25, 2002
Inventor(s):
Hoang, Brian

Title: METHOD OF TRANSFERRING DATA TO MULTIPLE UNITS OPERATING IN A LOWER-FREQUENCY DOMAIN

Examiner: Wong, W.
Group/Art Unit: 2668
Atty. Dkt. No: 5500-74100

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9/14/06
Date

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Further to the Notice of Appeal of July 17, 2006, Appellants present this Appeal Brief. Appellants respectfully request that this appeal be considered by the Board of Patent Appeals and Interferences.

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I. REAL PARTY IN INTEREST

The subject application is owned by Advanced Micro Devices, Inc., a corporation organized and existing under and by virtue of the laws of the State of Delaware, and having its principal place of business at One AMD Place, Sunnyvale, CA 94088, as evidenced by the assignment recorded at Reel 012545, Frame 0487.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are known which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-20 are pending in the present application. Claims 1-10 and 17-20 stand finally rejected and are the subject of this appeal. A clean copy of claims 1-10 and 17-20, as on appeal (incorporating all amendments), is included in the Appendix hereto.

IV. STATUS OF AMENDMEMNTS

No amendment to the claims has been filed subsequent to the final rejection. The Appendix hereto reflects the current state of the rejected claims.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a digital system including a plurality of ports (Fig. 4, 418-1, 418-2, page 5, line 7 to page 6, line 11) operating at a first clock rate, wherein each unit is configured to independently process a sequence of data items. The method further includes a domain crossover element (Fig. 4, 402 and 404-0 to 404-7, page 5, line 7 to page 6, line 11) configured to receive a stream of data items at a clock rate different from the first clock rate, and configured to distribute separate sequences of data items through separate ports to the plurality of units.

Independent claim 17 is directed to a method of distributing streams of data items receive at a first clock rate among a plurality of processing units operating at a second, slower clock rate. The method (see timing diagram, Fig. 5, page 6 line 12 to page 8, line 5) includes sequentially selecting one of a plurality of registers (Fig. 4, 404-0 to 404-8, page 5, line 7 to page 6, line 11) at the first clock rate. Each data item from the stream of data items is stored in a selected register as the data items are received. The method further includes selecting one of a first subset and one of a second subset of the plurality of registers, wherein said selecting is performed at the second clock rate, and wherein the second subset is distinct from the first. Data items are concurrently read from selected ones of the first and second subsets at the second clock rate.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APEAL

1. Claims 1-5 are rejected under 35 U.S.C. § 102(**b**) as being anticipated by Clauberg (U.S. Patent Number 6,389,018).

2. Claims 6-9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Clauberg in view of Chung (U.S. Patent Number 5,764,895).

3. Claim 10 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Clauberg in view of Johnson Counter (i.e. 5-Stage Johnson Counter), Talarek (U.S. Patent Number 6,628,679), and Segal (U.S. Patent Number 4,685,101).

4. Claims 17-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Clauberg in view of Talarek and Segal.

5. Claim 20 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Clauberg in view of Talearek and Segal and in further view of Kariquist (U.S. Patent Application Publication 2003/0063626).

VII. ARGUMENT

A. Claims 1-5

The Examiner rejected claims 1-5 as being anticipated by Clauberg under 35 U.S.C. § 102(b). Appellants respectfully traverse this rejection in light of the following remarks.

Clauberg fails to teach or suggest all of the elements of independent claim 1, which recites:

> "A digital system that comprises: a plurality of units operating at a first clock rate, each unit configured to independently process a sequence of data items; and a domain crossover element configured to receive a stream of data items at a second clock rate different from the first clock rate and configured to distribute **separate** sequences of data items through separate ports to the plurality of units" (emphasis added).

In the office action, the Examiner contends that Clauberg teaches plurality of units (Fig. 3C, 14.1/15.1 pair - 14.5/15.5 pair) operating at a first clock rate, each configured to independently process a sequence of data items, and a domain crossover element (Fig. 3C, demultiplexer 12) configured to receive a stream of data items at a second clock rate and configured to distribute separate sequences of data through separate ports to the plurality of units. Appellant respectfully disagrees with the Examiner's characterization of Clauberg, and submits that it does not teach a domain crossover element operating at a second clock rate different from a first clock rate at which a plurality of units operates.

Clauberg's system shown in Fig.'s 1 and 3A-3G, describes as a parallel processing unit, is simply a demultiplexer, a plurality of processing unit pairs, and a multiplexer. As described in Clauberg, the demultiplexer receives a stream of data items which are then

distributed to the processing unit pairs. The data items are processed in the pairs, progressing one step for each slot duration T, as shown in Fig.'s 3A-3G (it is noted that the slot duration T is the same slot duration T at which data items are received by demultiplexer 12). The sequence is then reassembled, in its original order by multiplexer 17, as Clauberg states in col. 5, lines 33-42:

> "At the right hand side of the parallel processing paths 13.1-13.5, the sub-streams--after having been processed--are fed into a multiplexer 17 employed to provide an output stream 18 of fixed length cells on the slotted output medium 19. This multiplexer 17 is designed such that the original sequence of the cells, i.e. the chronological order on the input medium 11, **is re-established**. This means that not only the order of cells (like in a FIFO device; first in first out) but also the **exact arrangement** within the slots is maintained." (Emphasis added)

Thus, while individual data items may be processed separately in the parallel processing unit of Clauberg, they are received thereby and distributed therefrom **serially**, in the same, **original** sequence.

In the 'Response to Arguments' section of the final office action, the Examiner contends that Clauberg describes the use of a set of parallel processing means which slows down the processing time when each set of processing elements within a processing path is considered as a whole (i.e. the total time it takes to process a demultiplexed cell has been slowed down). Appellant respectfully disagrees with the Examiner's characterization, and submits that the processing time **is not slowed down**, but is merely **divided** among several parallel processing paths. Furthermore, the processing time of an individual data item is **not slowed down**, contrary to the Examiner's assertion. Each cell shown in the examples given in Figs. 3A-3G **advances by one position for each T, i.e. by one position for each slot duration**. For example, cell A in Figs. 3A-3E advances to the demultiplexer (at time **T**) to processing unit 14.1 (at time **2T**) to processing unit 15.1 (at time **3T**) to the multiplexer (at time **4T**) to the slotted output medium (at time **5T**), or

in other words, advances one position for each T. After processing units 14.1 and 15.1 have completed there respective processing of cell A, **they undergo a plurality of idle cycles**, until cell F is processed by processing unit 14.1 **at time 7T**. In other words, processing units 14.1 and 15.1 (or for that matter, any of the processing units of Clauberg's parallel processing unit) **are not operating at a slower clock rate**, but rather, are experiencing **idle cycles** while operating at the **same clock rate at which cells were received by demultiplexer 12**. This clock rate also happens to be the same clock rate at which process data cells are received by multiplexer 17 and output therefrom. Furthermore, assembling the processed data cells for output from multiplexer 17 in the same sequence as they were received by demultiplexer 12 **and outputting one processed cell for each slot duration T would not be possible if the processing units were operating at a different clock rate than demultiplexer 12**.

Furthermore, considering the above, it is clear that Clauberg only teaches a single clock rate, wherein the clock period (the inverse of the rate) is one slot duration T. In col. 3, lines 44-46, Clauberg states:

> "The slotted character of the transmission medium is indicated by dividing up the time axis into slots. The slot duration is denoted by the letter `T`." (Emphasis added).

This is the only teaching or suggestion of a slot duration (and thus, a clock rate) by Clauberg, which makes **no distinction** between the slot duration for cells **entering** the parallel processing unit, **progressing through** the parallel processing unit, or **leaving** the parallel processing unit. Thus, Clauberg clearly teaches only a **single** clock rate, and thus does not teach a first clock rate and a second clock rate different from the first clock rate.

In the advisory action, the Examiner states, in item 1), that

"The examiner recites from the Response to Arguments of the last office action that the reference speaks of a different clock rate (col. 1, lines 40-46 and col. 2, lines 13-20), where EACH PARALLEL PROCESSING PATH SHOULD BE EVALUATED AS A WHOLE (i.e. the **total time** it takes for ENTIRE individual parallel processing path being at the first clock rate), the reason why the input processing is required to break down into sets of parallel processing paths." (Emphasis added).

However, as clearly shown in Fig.'s 3A-3G, the **total time** it takes to process any data cell in any of the parallel processing paths is 2T (i.e. 2 **slot durations**), with each individual processing unit performing its processing in **one slot duration (i.e. 1T),** and with the parallel path being experiencing at least 3T worth of idle slot durations before receiving another data cell for processing. Thus, even if one were to evaluate the processing paths as a whole, it does not change the fact that they operate at the **same clock rate as the demultiplexer** (and the multiplexer, for that matter). Rather, each processing path requires two clock cycles (i.e. two slot durations T) instead of one single clock cycle to complete processing, but nevertheless, **is operating at the same clock rate** as demultiplexer 12. This clock rate is **not** changed by the fact that data items may be processed in parallel nor is the clock rate changed by the fact that individual processing units within the parallel processing unit may experience idle cycles in which they are not processing any data item, nor is the clock rate changed by the fact that each parallel processing path requires **multiple slot durations** (i.e. clock cycles) to complete processing. **Thus, even when considering the parallel processing paths as a whole, the clock rate for all operations in the system of Clauberg is clearly the inverse of one slot duration, or 1/T.**

With regard to the Examiner's citations noted above, col. 1, lines 40-46 of Clauberg states:

"The higher the data transmission rate in a cell based system (e.g. an ATM system) is, the faster certain operations must be performed on the cells. On-the-fly cell processing which usually requires that all operations are completed within a given number of clock cycles (corresponding to the time until the next cell on the slotted medium arrives) is getting difficult, if not even impossible",

while col. 2, lines 13-20 of Clauberg states:

"According to the present invention, the consecutive fixed length cells on a slotted medium are assigned to N parallel, identical processing paths each of which comprise one or more processing units. Due to this, the number of clock cycles available to such a Processing unit is multiplied by N if only each (N+1)-th cell is processed by the same processing path. This introduces N virtual but identical data processing paths." (Emphasis added).

Neither of the above citations discusses first and second clock rates that are different from each other. The first of these citations describes the problem of the difficulty of cell processing in a given number of clock cycles – a problem that **would not** be solved by operating the demultiplexer at a clock rate greater than that of the processing units of Fig. 1 and Fig.'s 3A-3G (Appellant notes that claim 2 recites the second clock rate as being greater than the first clock rate). The second of the citations, describing the system of Clauberg, is directed to increasing the number of available clock cycles for processing data, but provides no teaching or suggestion of a first clock rate and a second clock rate that is different from the first, much less wherein the second clock rate is greater than the first.

The Examiner further states, in item 2) of the advisory action, the Examiner states

".. the reference used teaches that the cells are being "re-established" to a same sequence at the end of the system, alluding to the first and second clock rates

being identical. The examiner asserts that the applicant is referring to fig. 3, #17 of the reference, but the examiner is using only a portion of the system (fig. 3, 30, 12, and 13.x) against the applicant's system (see fig. 1) and rejecting the argued claim 1." (Emphasis added).

Regardless of whether the Examiner is using the entire system of Clauberg or only a portion thereof, it does not change the fact that the clock rate at which cells progress through the parallel processing unit (1/T) is the same as the clock rate at which cells are received by demultiplexer 12 thereof.

These teachings of Clauberg are clearly in contrast to Appellant's independent claim 1, which recites a plurality of units operating at a **first** clock rate and a domain crossover element configured to receive a stream of data items at a **second** clock rate **different** from the first clock rate. These limitations are supported in Applicant's specification in Figs. 4 and 5 and the descriptions related thereto. More particularly, Fig. 4 illustrates a plurality of units (e.g. 418-1, 418-2) which operate at a first clock rate (the rate of the *clock out* signal) and a domain crossover element (e.g., 402 and 404-0 to 404-7) configured to receive a stream of data items at a second clock rate (the rate of the *clock in* signal). Fig. 5 illustrates a first clock signal operating at a first clock rate (test.queue0.YCLK) and a second clock signal operating at a second clock rate (test.queue0.XCLK), wherein the second clock rate in this example is twice the first clock rate

For at least these reasons, Appellant submits that Clauberg fails to teach or suggest a plurality of units operating at a first clock rate and a domain crossover element operating at a second clock rate different from the first clock rate, as recited in claim 1. Appellant further submits that for at least theses reasons Clauberg fails to teach or suggest wherein the second clock rate is greater than the first clock rate, as recited in claim 2. Accordingly, a case of anticipation has not been established, and thus reversal of the Examiner's rejection is respectfully requested.

B. **Claims 6-9**

The Examiner rejected claims 6-9 as being unpatentable over Clauberg in view of Chung under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Claims 6-9 depend from claim 1, and thus incorporate its features. In making the rejection, the Examiner states "Regarding claim 6, Clauberg describes all the limitations set forth in claim 1" (e.g., see final office action). As noted above, the Examiner states, in item 1) of the advisory action, that:

> "The examiner recites from the Response to Arguments of the last office action that the reference speaks of a different clock rate (col. 1, lines 40-46 and col. 2, lines 13-20), where EACH PARALLEL PROCESSING PATH SHOULD BE EVALUATED AS A WHOLE (i.e. the **total time** it takes for ENTIRE individual parallel processing path being at the first clock rate), the reason why the input processing is required to break down into sets of parallel processing paths." (Emphasis added).

However, in item 2) of the Advisory Action, the Examiner states that:

> "... the reference used teaches that the cells are being "re-established" to a same sequence at the end of the system, alluding to the first and second clock rates being identical. The examiner asserts that the applicant is referring to fig. 3, #17 of the reference, but the **examiner is using only a portion of the system (fig. 3, 30, 12, and 13.x) against the applicant's system** (see fig. 1) and rejecting the argued claim 1." (Emphasis added).

Thus, it appears that in considering the features of claim 1 in the rejection of claims 6-9, the Examiner is considering the parallel processing paths taught by Clauberg as a whole,

but is **not** considering **the system** taught by Clauberg **as a whole**. As such, Appellant respectfully submits that the Examiner's § 103(a) rejection of claims 6-9 **is improper** in light of **MPEP 2142.02(VI), which clearly states that the prior art must be considered in its entirety, including disclosures that teach away from the claims.**

Appellant submits that Clauberg teaches away from independent claim 1, and thus, teaches away from the combinations of features recited in each of claims 6-9. As noted above, the system taught by Clauberg is configured to receive a sequence of data cells, process data cells in parallel processing paths, and then reestablish and distribute the cells in the same sequence as they were originally received. Appellant further noted that each cell progresses one step through the system of Clauberg for each **slot duration T**, with **T** being the slot duration for both receiving the cells in demultiplexer 12 and distributing them in the same sequence from multiplexer 17. When considering that the cells are received and distributed in the same sequence in Clauberg's system, Appellant submits that **Clauberg teaches away from the distribution of separate sequences.** Furthermore, considering that a cell progresses one step through Clauberg's system for each slot duration T (i.e. at a clock rate of 1/T), Appellant submits that Clauberg teaches away from any combination **that would include a plurality of units operating at a first clock rate, and a domain crossover element configured to receive a stream of data items at a second clock rate different from the first clock rate**. Thus, in the Examiner's apparent failure to consider the **entirety** of Clauberg's system, as noted in item 2) of the Advisory Action ("The examiner asserts that the applicant is referring to fig. 3, #17 of the reference, but the examiner is using only a portion of the system"), Appellant submits that the § 103(a) rejection of claims 6-9 is improper, as he has not met the requirements of MPEP 2142.02(VI).

Furthermore, as noted above, given that all operations in Clauberg's system are timed to a slot duration T (**and thus, a clock rate of 1/T**), Appellant submits that **the cited references, taken singly in combination, fail to teach or suggest all of the elements of the independent claims.**

For at least these reasons, as well as those given above in regard to claim 1, Appellant submits that a case of obviousness has not been established for claims 6-9, and further submits, that the § 103(a) rejection is improper for failing to consider the prior art in its entirety, including those disclosures that teach away from the claims. Accordingly, reversal of the Examiner's rejection is respectfully requested.

C. Claim 10

The Examiner rejected claim 10 as being unpatentable over Clauberg in view of Johnson Counter under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Claim 10 depends from claim 1, and thus incorporates its features. In making the rejection, the Examiner states, regarding claim 10, "Clauberg describes all the limitations set forth in claim 1" (e.g., see final office action). As noted above, the Examiner states, in item 1) of the advisory action, that:

> "The examiner recites from the Response to Arguments of the last office action that the reference speaks of a different clock rate (col. 1, lines 40-46 and col. 2, lines 13-20), where EACH PARALLEL PROCESSING PATH SHOULD BE EVALUATED AS A WHOLE (i.e. the **total time** it takes for ENTIRE individual parallel processing path being at the first clock rate), the reason why the input processing is required to break down into sets of parallel processing paths." (Emphasis added).

However, in item 2) of the Advisory Action, the Examiner states that:

> "... the reference used teaches that the cells are being "re-established" to a same sequence at the end of the system, alluding to the first and second clock rates

being identical. The examiner asserts that the applicant is referring to fig. 3, #17 of the reference, but the **examiner is using only a portion of the system** (fig. 3, 30, 12, and 13.x) **against the applicant's system** (see fig. 1) and rejecting the argued claim 1." (Emphasis added).

Thus, it appears that in considering the features of claim 1 in the rejection of claim 10, the Examiner is considering the parallel processing paths taught by Clauberg as a whole, but is **not considering the system taught by Clauberg as a whole**. As such, Appellant respectfully submits that the Examiner's § 103(a) rejection of claim 10 **is improper** in light of **MPEP 2142.02(VI), which clearly states that the prior art must be considered in its entirety, including disclosures that teach away from the claims.**

Appellant submits that Clauberg teaches away from independent claim 1, and thus, teaches away from the combinations of features recited in claim 10. As noted above, the system taught by Clauberg is configured to receive a sequence of data cells, process data cells in parallel processing paths, and then reestablish and distribute the cells in the same sequence as they were originally received. Appellant further noted that each cell progresses one step through the system of Clauberg for each **slot duration T**, with **T** being the slot duration for both receiving the cells in demultiplexer 12 and distributing them in the same sequence from multiplexer 17. When considering that the cells are received and distributed in the same sequence in Clauberg's system, Appellant submits that **Clauberg teaches away from the distribution of separate sequences.** Furthermore, considering that a cell progresses one step through Clauberg's system for each slot duration T (i.e. at a clock rate of 1/T), Appellant submits that Clauberg teaches away from any combination **that would include a plurality of units operating at a first clock rate, and a domain crossover element configured to receive a stream of data items at a second clock rate different from the first clock rate**. Thus, in the Examiner's apparent failure to consider the **entirety** of Clauberg's system, as noted in item 2) of the Advisory Action ("The examiner asserts that the applicant is referring to fig. 3, #17 of the reference, but the examiner is using only a portion of the system"),

Appellant submits that the § 103(a) rejection of claims 6-9 is improper, as he has not met the requirements of MPEP 2142.02(VI).

Furthermore, as noted above, given that all operations in Clauberg's system are timed to a slot duration T **(and thus, at a clock rate of 1/T)**, Appellant submits that **the cited references, taken singly in combination, fail to teach or suggest all of the elements of the independent claims.**

For at least these reasons, as well as those given above in regard to claim 1, Appellant submits that a case of obviousness has not been established for claim 10, and further submits, that the § 103(a) rejection is improper for failing to consider the prior art in its entirety, including those disclosures that teach away from the claims. Accordingly, reversal of the Examiner's rejection is respectfully requested.

D. Claims 17-19

The Examiner rejected claims 17-19 as being unpatentable over Clauberg in view of Johnson Counter, Talerek and Segal under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

The Examiner has improperly rejected claims 17-19 under 35 U.S.C. § 103(a), as he has failed to consider the prior art in its entirety per MPEP 2142.02(VI). Clauberg teaches away from the independent claims, while the combination/modification proposed by the Examiner would change the principle of operation of Clauberg.

Appellant's independent claim 17 recites, in pertinent part:

"sequentially selecting one of a plurality of registers at the first clock rate ... sequentially selecting one of a first subset of the plurality of registers at the second

clock rate; sequentially selecting one of a second subset of the plurality of registers at the second clock rate, wherein the second subset is distinct from the first subset; and **concurrently** reading data items from the selected ones of the first and second subsets at the second clock rate"

In item 3) of the Advisory Action, the Examiner states:

"On p. 10-11, the applicant argues: the references of Segal and [Clauberg] was not suggested to be combined, nor are compatible to be combined (teaches away [from] the other reference) for the same argument a (2) above. The examiner noted that a proper motivation has [been] provided to combined the references of Segal and [Clauberg]. For the same response as (2) above **(i.e. using only a portion of the system from the reference** to match the applicant's system of fig. 1), the examiner asserts that the references of Segal and [Clauberg] can be combined." (Emphasis added)

On pages 10-11 of the final office action response, Appellant presented arguments regarding claims 17-19. In light of the above remarks, it appears that the Examiner is **acknowledging** that he is **not considering the prior art reference** of Clauberg **in its entirety**, i.e. **as a whole**. As previously noted, Clauberg states, in col. 5, lines 33-42:

"At the right hand side of the parallel processing paths 13.1-13.5, the sub-streams--after having been processed--are fed into a multiplexer 17 employed to provide an output stream 18 of fixed length cells on the slotted output medium 19. This multiplexer 17 is designed such that the original sequence of the cells, i.e. the chronological order on the input medium 11, **is re-established**. This means that not only the order of cells (like in a FIFO device; first in first out) but also the **exact arrangement** within the slots is maintained." (Emphasis added)

In the final office action response, Appellant argued that combining Segal with Clauberg (with or without Talarek) in the manner proposed by the Examiner would change the principle of operation of re-establishing the chronological order of the cells and distributing them in the exact arrangement within the slots as they were first received. Appellant argued that the chronological order of cells could not be re-established, nor could cells be distributed in their exact arrangement within the slots if they were to be **concurrently** read from selected ones of the first and second subsets, as similarly recited in claim 17.

In response, the Examiner's statement in item 3) is that **only a portion of** Clauberg's system **is being considered** in making the rejection, and thus is not considering Clauberg **as a whole**, as required by MPEP 2142.02(VI). As such, Appellant respectfully submits that the **Examiner's § 103(a) rejection of claim 17-19 is improper** in light of **MPEP 2142.02(VI), which clearly states that the prior art must be considered in its entirety, including disclosures that teach away from the claims.**

Notwithstanding the above, Appellant submits that Clauberg teaches away from independent claim 17. As noted above, independent claim 17 includes the recitation of "**concurrently** reading data items from the selected ones of the first and second subsets at the second clock rate" (emphasis added). Consideration of Clauberg's system as a whole would include consideration that multiplexer 17 of parallel processing unit 9 distributes cells in an output stream in the same chronological order in which they were received by demultiplexer 12. However, Clauberg's teaching of re-establishing the original sequence of cells in the chronological order in which they were received would not be possible if the were to be read **concurrently** from selected ones of first and second subsets, as multiplexer 17 can pass only one input in a given time slot. Distributing the cells in chronological order on a single slotted output medium 19 suggests that the cells must be read and place upon the output medium in chronological order, i.e. one at a time. **Accordingly, Appellant submits that Clauberg's teaching of reestablishing the chronological order of the cells and distributing them from the parallel processing**

unit in the exact arrangement within the slots as they were first received teaches away from concurrently reading data items from selected ones of the first and second subsets, as recited in claim 17.

Appellant further submits that combination proposed by the Examiner would change the principle of operation of the Clauberg reference. In the final office action, the Examiner states:

> "Clauberg and Talarek combined lack what [the] Segal describes: ... concurrently reading data items from the selected ones of the first and second subsets [at the second clock rate]" (emphasis added).

Thus, the Examiner proposes combining Segal with Clauberg and Talarek to remedy the deficiency wherein the latter two references fail to teach or suggest concurrently reading data items from selected ones of the first and second subsets. When considering the Clauberg reference as a whole, multiplexer 17 of parallel processing unit 9 distributes cells in an output stream in the same chronological order in which they were received by demultiplexer 12. Thus, Clauberg's principle of operation includes parallel processing unit 9 receiving cells in a certain chronological order and distributing the cells therefrom in the same chronological order. However, modifying Clauberg in the manner proposed by the Examiner, wherein data items would be read from first and second subsets of registers concurrently would change the principle of operation of Clauberg's parallel processing unit. More particularly, the concurrent reading of data items would change Clauberg's principle of re-establishing the chronological order of cells (as received on the input medium) like in a FIFO device, and their exact arrangement within the slots for distribution on the slotted output medium. **MPEP 2143.01(VI.) states that the proposed modification cannot change the principle of operation of a reference, and further states that if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified (in this case, Clauberg), then the teaching of the references are not sufficient to render**

the claims *prima facie* obvious. Accordingly, since the modification of Clauberg proposed by the Examiner would change the principle of operation of Clauberg's parallel processing unit, Appellant submits that the teachings of the references are not sufficient to render the claims obvious.

Thus, since the Examiner has failed to consider the Clauberg reference as a whole, since Clauberg teaches away from independent claim 17, and since the proposed modification would change the principle of operation of Clauberg's parallel processing unit, Appellant respectfully submits that the Examiner's rejection of claims 17-19 under 35 U.S.C. § 103(a) is erroneous. Accordingly, reversal of the Examiner's rejection is respectfully requested.

E. Claim 20

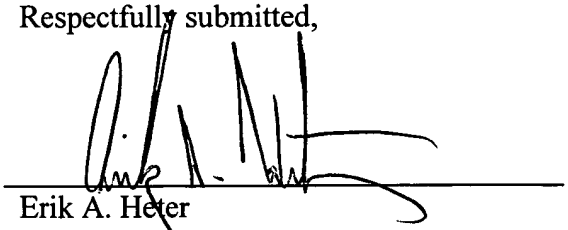
The Examiner rejected claim 20 as being unpatentable over Clauberg, in view of Talarek, Segal, and Kariquist under 35 U.S.C. § 103(a). Appellants respectfully traverse this rejection in light of the following remarks.

Appellant notes that claim 20 depends from independent claim 17. Accordingly, for at least the same reasons stated above, Appellant submits that the Examiner has improperly rejected claim 20 by failing to consider the prior art in its entirety per MPEP 2142.01(VI), that Clauberg teaches away from claim 20 (by virtue of teaching away from claim 17), and that the combination proposed by the Examiner would change Clauberg's principle of operation. Accordingly, Appellant respectfully requests reversal of the Examiner's § 103(a) rejection of claim 20.

VII. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejection of claims 1-10 and 17-20 was erroneous, and reversal of his decision is respectfully requested.

Respectfully submitted,



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IX. APPENDIX

The claims on appeal are as follows.

1. A digital system that comprises:

a plurality of units operating at a first clock rate, each unit configured to independently process a sequence of data items; and

a domain crossover element configured to receive a stream of data items at a second clock rate different from the first clock rate and configured to distribute separate sequences of data items through separate ports to the plurality of units.

2. The system of claim 1, wherein the second clock rate is greater than the first clock rate, and wherein the number of ports equals a positive integer multiple of the ratio of the second clock rate to the first clock rate.

3. The system of claim 2, wherein said number of ports is two.

4. The system of claim 1, wherein the units are general purpose processors.

5. The system of claim 1, wherein the data items are data packets having fields for a packetID, a targetID, Control flags, and packet Data.

6. The system of claim 1, wherein the domain crossover element includes a circular buffer having a plurality of distinct sections each associated with a corresponding one of the separate ports, and each having N storage locations, where N is a positive integer.

7. The system of claim 6, wherein each of said separate sequences of data items is formed by repeatedly reading from sequential storage locations in a corresponding section of the circular buffer.

8. The system of claim 6, wherein N is two or greater.

9. The system of claim 7, wherein N is four.

10. The system of claim 1, wherein the domain crossover element comprises:

a counter/decoder that receives an input clock and responsively asserts sequential ones of a plurality of output signals;

a plurality of storage location registers, each coupled to receive corresponding one of the plurality of output signals from the counter/decoder, and each coupled to receive a stream of input data items, wherein each of the storage location registers is configured to store an input data item when the corresponding one of the plurality of output signals is asserted;

a plurality of multiplexers each configured to provide a sequence of data items to one of the separate ports, wherein each of the multiplexers is coupled to storage location registers associated with said one of the separate ports; and

an output counter that receives an output clock, wherein the output counter is coupled to one or more of the multiplexers and configured to sequentially select storage locations for the one or more multiplexers to access to provide said sequences of data items.

17. A method of distributing a stream of data items received at a first clock rate among a plurality of processing units operating at a second, slower clock rate, the method comprising:

sequentially selecting one of a plurality of registers at the first clock rate;

storing each data item from the stream of data items in a selected register as the data items are received;

sequentially selecting one of a first subset of the plurality of registers at the second clock rate;

sequentially selecting one of a second subset of the plurality of registers at the second clock rate, wherein the second subset is distinct from the first subset; and

concurrently reading data items from the selected ones of the first and second subsets at the second clock rate.

18. The method of claim 17, wherein the first data item read from the first subset is read at a different time than the first data item read from the second subset.

19. The method of claim 17, wherein all registers in the second subset are written after all registers in the first subset.

20. The method of claim 17, further comprising:

continuously repeating the acts of claim 17 while a reset signal is de-asserted

X. EVIDENCE APPENDIX

No evidence submitted under 37 C.F.R. §§ 1.130, 1.131, or 1.132 or otherwise entered by the Examiner is relied upon in this appeal.

XI. RELATED PROCEEDINGS APPENDIX

There are no related proceedings.

Application No.: 10/057,393
Filed: January 25, 2002
Inventor(s):
Hoang, Brian

Title: METHOD OF TRANSFERRING DATA TO MULTIPLE UNITS OPERATING IN A LOWER-FREQUENCY DOMAIN

§

Examiner: Wong, W.
Group/Art Unit: 2668
Atty. Dkt. No: 5500-74100

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Erik A. Heter
Printed Name

Signature

September 14, 2006
Date

FEE AUTHORIZATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The Commissioner is hereby authorized to charge the following fee to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account Number 50-1505/5500-74100:

Fee:	Appeal Brief
Amount:	$500.00
Attorney Docket No.:	5500-74100

The Commissioner is also authorized to charge any extension fee or other fees which may be necessary to the same account number.

Respectfully submitted,

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